REMARKS/ARGUMENTS

Claims 1-15 are pending in the present application. By this reply, claims 5-15 have been added. Claims 1, 2 and 11 are independent claims

The specification and claims have been revised to correct informalities and to clarify the invention according to U.S. practice. These modifications are fully supported by the original disclosure and do not add any new matter.

Abstract

At the Examiner's request, a new Abstract is provided.

Disclosure and Claim Objection

The disclosure and claims have been objected to because of minor informalities. Accordingly, the specification and claims have been reviewed and revised to correct these informalities as suggested by the Examiner. Thus, the objection should be withdrawn.

35 U.S.C. § 112, Second Paragraph, Rejection

Claims 1 and 4 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. These claims have been revised to clarify the invention. Accordingly, the rejection is moot and must be withdrawn.

35 U.S.C. § 103 Rejections

Claims 1-4 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's disclosed background art[1] in view of Davis et al. (U.S. Patent No. 6,505,222). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

Regarding independent claims 1 and 2, the Examiner alleges that Applicant's disclosed background art teaches the claimed invention except for the feature of taking the absolute value of the real part and the imaginary part of the first error calculated by the DD slicer and summing these absolute values to produce a sum.

To correct this deficiency of Applicant's disclosed background art, the Examiner further relies on Davis et al. Particularly, the Examiner alleges that Davis et al. teaches the feature of taking the absolute value of the real part and the imaginary part of the first error calculated by DD slicer and summing these absolute values.

However, in Davis et al., as shown in Fig. 4, the absolute value unit 127 takes the absolute value of the error signal generated by the adder 126. In clear contrast, in Applicant's embodied invention, the present inventor has defined obtaining the absolute value of the error as taking the absolute value of the real part and the imaginary part of the first error calculated from the DD

[1] It is not known whether Applicant's disclosed background art has a proper date to be used as a reference to reject the present claims under 35 U.S.C. § 103. Applicant will still address the rejection(s) assuming that it is for the sake of the argument, but reserves the right to traverse the rejection(s) based on the proper date ground.

slicer and summing these absolute values. This teaching is completely missing from Davis et al. The Examiner should note that the absolute value of an error signal (Davis et al.) is not the same as the sum of the absolute value of a real part of the error signal and the absolute value of an imaginary part of the error signal (Applicant). These are mathematically different operations producing completely different results and thus, cannot and must not be equated to each other.

Furthermore, there is no motivation to replace the DD error size calculation unit 40 of Applicant's background Fig. 1 with the feature of obtaining the absolute value of the error signal by the absolute value unit 127 of Davis et al., which is suggested by the Examiner. In Davis et al., the output of the absolute value unit 127 is used to provide bias control using the bias control system 90, which is separate from the functions and operations of the equalizer 84 of Davis et al. In total contrast, in Applicant's background art as shown in Fig. 1, the output of the DD error size calculation unit 40 is multiplied by the Sato error multiplied by a scale constant k_2, in the multiplier 70. The output of the multiplier 70 is then added to the DD error multiplied by a scale constant k_1 to produce an inverse response signal of a channel *by the equalizer*. Thus, since the use of the output of the absolute value unit 127 of Davis et al. is completely different from the use of the sum (output of the DD error size calculation unit 40) in Applicant's background art, there is absolutely

no reason to replace the DD error size calculation unit 40 of Applicant's background Fig. 1 with the absolute value unit 127 of Davis et al.

But even if the references were combinable, assuming *arguendo*, the combination of reference would still fail to teach or suggest the feature of taking the absolute value of the real part and the imaginary part of the first error calculated from the DD slicer and summing these absolute values, as required by the independent claim, because Davis et al. merely teaches that the absolute value unit 127 takes the absolute value of the error signal and nothing more as discussed above.

Accordingly, the invention as recited in independent claims 1 and 2 and their dependent claims (due to their dependency) is patentable over the applied references, and the rejection must be withdrawn.

New Claims

Claims 5-10 depend from independent claims 1 and 2 and are thus allowable at least for the same reasons that these independent claims are allowable as discussed hereinabove. Claims 11-15 contain similar subject matter as claims 1 and 5-9, and are thus believed to be allowable based on the same reasons that claims 1 and 5-9 are allowable as discussed herein.

CONCLUSION

For the foregoing reasons and in view of the above clarifying amendments, Applicant respectfully requests the Examiner to reconsider and withdraw all of the objections and rejections of record, and earnestly solicits an early issuance of a Notice of Allowance.

Should there be any outstanding matters which need to be resolved in the present application, the Examiner is respectfully requested to contact Esther H. Chong (Registration No. 40,953) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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JTE/EHC:lmh
Attachments: Abstract of the Disclosure
Substitute Specification
Mark-Up Copy of Sub. Specification

ERROR CONTROL APPARATUS AND METHOD FOR CHANNEL EQUALIZER

BACKGROUND OF THE INVENTION

1. Field of the Invention

[001] The present invention relates to an error control method for a digital channel equalizer, and more particularly, to an error control method for a channel equalizer which is capable of improving complexity and error update speed by decreasing the number of gates of a ~~DD~~ Decision-Directed (DD) error size calculation unit of a combined G-pseudo channel equalizer among digital channel equalizers.

2. Description of the Background Art

[002] Generally, a channel equalizer is an apparatus for decreasing bit detection error by compensating for a restricted bandwidth of a plurality of filters used in a sending/receiving end and a distortion generated while a signal passes through multiple paths of a transmission channel, when a digital transmission system such as a HDTV sends/receives a signal.

[003] If the signal transmitted from the sending end is distorted, contains noise, and has a higher signal level, the error generation rate is increased. Thus, the receiving end utilizes a channel equalizer in order to accurately restore a transmitted signal by compensating for the distortion of a received signal.

[004] The operation of the channel equalizer is divided into an acquisition step of acquiring a signal close to the original signal by reducing error until a distorted, received signal is compensated to ~~thus~~ be close to the original signal, and a tracking step of configuring the signal whose error is reduced until it becomes

close to the original signal so that it meets changes in channel well. Even after the received signal is compensated for, if the signal sent from the sending end is seriously distorted, there occurs a problem that the equalizer diverges. This problem can be overcome by inserting a predetermined training sequence signal into the signal transmitted from the sending end to the receiving end and transmitting the same.

[005] When the training sequence signal is inserted into the transmission signal, the bandwidth of a signal to be transmitted is reduced since the training sequence signal is a signal for correcting an error, and the complexity of the sending end system is increased since an apparatus for generating the training sequence must be added to the sending end system.

[006]~~,~~

Therefore, a blind channel equalizer~~,~~ such as a combined G-pseudo channel equalizer which has an excellent convergence characteristic even if the training sequence signal is not inserted, has been researched and developed.

[007] The combined G-pseudo channel equalizer is an equalizer combining an equalizer utilizing a DD algorithm and an equalizer utilizing a Sato algorithm, each having a DD slicer and a Sato slicer. In the case that a signal received by the G-pseudo channel equalizer is updated by a DD error only, the equalizer is easy to diverge. Thus, convergence is performed by using both DD error and Sato error. In addition, in the case that an error of a signal received by using a Sato error only is updated, there remains a lot of residual errors even after the final convergence. Thus, errors can be reduced by performing convergence using a DD error at the point of time where the convergence is performed to a certain extent.

[008] In the case that a transmission signal to which the training sequence signal is not inserted is inputted, the DD error is an error detected by estimating an

approximate value of the original signal from the above input signal, ~~and, on the contrary,~~ whereas the Sato error is an error detected from the original signal by the mean power of the inputted signal.

[009] Figure 1 is a block diagram of a combined G-pseudo channel equalizer according to the conventional art, which ~~including:~~ includes an equalizer filter 10 for correcting an error of received data; a DD(Decision-Directed) slicer for generating a DD error upon receipt of a correction signal outputted from the equalizer filter 10; a DD error size calculation unit 40 for calculating the size of the outputted DD error; ~~and~~ a Sato slicer unit 50 for calculating the Sato error upon receipt of the correction signal outputted from the equalizer filter 10; multipliers 30, 60, 70; and an adder 80.

[010] ~~.~~

The operation of the thusly constructed combined G-pseudo channel equalizer will be described with reference to Figures 1 and 2.

[011] If the signal sent from the sending end is inputted to the channel equalizer via a channel without the training sequence signal, the channel equalizer obtains the optimum value of ~~a~~ an inverse response of the channel, ~~said~~ this optimum value generating the original signal transmitted from the sending end by multiplying the original signal and the response value of the channel at the output end of the channel equalizer.

[012] The mathematical formula for obtaining the above-described transmitted original signal will be expressed as follows.

$a \cdot s \cdot s^{-1} = a$ ---------- (1)

a is the original signal.

s is the response value of the channel.

s^{-1} is the optimum value of the inverse response of the channel.

[013] If the signal a is inputted to the equalizer filter 10, the optimum value of

the inverse response (~~s~~(s^{-1}) of the channel is outputted by correcting an error of the received signal by the equalizer filter 10. The outputted signal is obtained by correcting an error by the DD slicer unit 20 and the Sato slicer unit 50.

[014] In the DD slicer unit 20, a DD silcer 21 ~~calculates~~ performs calculation on the inputted signal to output the most approximate value of the original signal, and an abstractor 22 abstracts the value outputted from the equalizer filter 10 from the outputted approximate value to thus generates a DD error. The generated DD error is multiplied by a scale constant k_1 by the multiplier 30 to be automatically converted into the Sato error mode.

[015] In the Sato slicer unit 50, a Sato slice 51 ~~calculates~~ performs calculation on the inputted signal to output the normal value of the inputted value, and an abstractor 52 abstracts the value outputted from the equalizer filter 10 from the calculated normal value to thus generate an Sato error. The generated Sato error is multiplied by a scale constant k_2 by the multiplier 60 to be automatically converted into the DD error mode.

[016] Even if the point of time where the Sato error mode and the DD error mode are converted is not set, the generated DD error and the generated Sato error are automatically converted into the Sato error mode and the DD error mode, respectively.

[017] Figure 2 is a graph comparing the characteristics of a general Sato error and the characteristics of a general DD error. While the DD error has a white value, i.e., a uniform value, the inverse response of the channel obtained from the combined G-pseudo channel equalizer, i.e., a G-pseudo error, is reduced by means of a Sato error. However, at point t_1 of time in a certain section, the Sato error becomes uniform. Since then, the G-pseudo error is reduced by means of the DD error.

[018] The Sato error has a considerable error value even after it has converged on the optimum point, i.e., until the equalizer ~~become~~ outputs a signal close to the optimum value of the inverse response s^{-1} of the channel. Thus, if the DD error and the Sato error are added, the G-pseudo error has an error value as much as the Sato error even though the DD error has an error value of almost 0. This is the limitation on the blind method.

[019] For this reason, if the Sato error multiplied by the scale constant is multiplied by the absolute value of the DD error calculated in the DD error size calculation unit 40, the DD error has a white value, i.e., a uniform value in the first section where the optimum value of the inverse response s^{-1} is searched for, thereby not affecting the G-pseudo error. At this time, the G-pseudo error is reduced by the Sato error. However, as the Sato error ~~become~~ becomes uniform in the section t_1, i.e., it converges on 0 in the section t_1, the G-pseudo error value is reduced by the DD error value. Thus, the optimum value of the inverse response of the channel can be searched for by means of the DD error only.

[020] The above described coefficient updating equation and filter output equation can be expressed as follows.

$$C_{k+1} = C_k + \mu D_k^* e_k^G \quad \text{---------- (2)}$$

$$Y(n) = \sum D^T C \quad \text{---------- (3)}$$

$$e_k^G = k_1 e_k + k_2 |e_k| e_k^S \quad \text{---------- (4)}$$

$$|e_k| = \sqrt{e_1^2 + e_Q^2} \quad \text{---------- (5)}$$

C_{k+1} is a coefficient of a filter tab of an equalizer of the next time.

C_k is a coefficient of a filter tab of an equalizer of the current time.

is the size of a step.

D_k is a data stored in the filter tab of the current time.

e_k^G is a G-pseudo error of the current time.

e_K^S is a Sato error of the current time.

e_k is a DD error of the current time.

k_1 and k_2 are scale constants.

e_I is a real error.

e_Q is an imaginary error.

[021] The value obtained by multiplying the Sato error by a scale constant k_2 is multiplied by the value $|e_k|$ calculated in the DD error calculation unit 40, and then the resultant value $|e_k|e_k^S$ is added to the value obtained by multiplying the DD error by the scale constant k_1, for thereby obtaining the optimum value s^{-1} of the G-pseudo equalizer.

[022] The optimum value s^{-1} obtained by the G-pseudo channel equalizer performs convergence well in most channel environments. However, since the value $|e_k|$ calculated in the DD error calculation unit 40 is the square root of the sum of a real error square and an imaginary square, i.e., $\sqrt{e_I^2 + e_Q^2}$, the complexity of the DD error calculation unit 40 ~~becomes higher~~ is increased. In the case that the DD error calculation unit 40 is ~~hardwarically~~ implemented, a large number of gates are required, for thereby increasing the size thereof and the complexity. In addition, it takes much time to obtain the square root ~~to thus degrade~~, which degrades the performance of a receiver.

SUMMARY OF THE INVENTION

[023] Accordingly, it is an object of the present invention to provide an error control method for a channel equalizer which reduces the number of gates needed in the equalizer by modifying the structure of a DD error size calculation unit while maintaining the performance of a combined G-pseudo channel equalizer and improves the performance of a receiver by enhancing error update speed.

[024] It is another object of the present invention to provide a channel equalizer that overcomes the limitations and problems of the background art.

[025] To achieve the above ~~object~~ and other objects, there is provided a channel equalizer according to the present invention, which includes: an equalizer filter for correcting an error upon receipt of a signal transmitted by a sending end; a DD slicer for calculating a first error upon receipt of the corrected signal from the equalizer filter; a Sato slicer for calculating a second error upon receipt of the corrected signal from the equalizer filter; and a DD error size calculation unit for taking the absolute value of the real part and imaginary part of the first error calculated from the DD slicer, summing them, and then obtaining the absolute value of the error.

[026] To achieve the above ~~object~~ and other objects, there is provided an error control method for a channel equalizer according to the present invention, which includes the steps of: multiplying a first error calculated from a DD slicer and a second error calculated from a Sato slicer each by a scale constant; taking the absolute value of the real part and imaginary part of the first error calculated from the DD slicer, summing them, and then obtaining the absolute value of the first error; obtaining the absolute value of an inverse response signal of a channel by multiplying the absolute value of the first error by the second error multiplied by the scale constant and adding the resultant value to a first error multiplied by the scale constant; and generating a filter tab coefficient to reproduce a signal transmitted from a sending end by feeding back the absolute value of the inverse response of the channel signal to the equalizer filter.

[027] Additional advantages, objects and features of the invention will become more apparent from the description which follows.

BRIEF DESCRIPTION OF THE DRAWINGS

[028] The present invention will become better understood with reference to the accompanying drawings which are given only by way of illustration and thus are not limitative of the present invention, wherein:

[029] Figure 1 is a block diagram illustrating elements of a combined G-pseudo channel equalizer according to the conventional art;

[030] Figure 2 is a graph comparing the characteristics of a general Sato error and DD error;

[031] Figure 3 is a block diagram illustrating elements of a combined G-pseudo channel equalizer according to the present invention; and

[032] Figure 4 is an exemplary view comparing the error distribution by means of the absolute value of a DD error according to the conventional art and the error distribution by means of the absolute value of a DD error according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[033] The preferred ~~embodiment~~ embodiments of the present invention will now be described with reference to the accompanying drawings.

[034] Figure 3 is a block diagram illustrating elements of a combined G-pseudo channel equalizer according to an embodiment of the present invention. The channel equalizer includes: an equalizer filter 100 for correcting an error of a received signal; a DD slicer unit 200 for generating a DD error by means of the approximate value of a signal outputted from the equalizer filter 100; a DD error size calculation unit 400 for calculating the size of the DD error; and a Sato slicer unit 500 for outputting a Sato error by means of the average value of the signal outputted from the equalizer filter.

[035] The operation of the elements of the channel equalizer according to the invention will be explained with reference to Figures 2, 3, and 4.

[036] If a signal sent from a sending end is transmitted to the combined G-pseudo channel equalizer via a channel, the equalizer calculates the optimum value of the inverse response of the channel in order to compensate the original signal. If the signal transmitted from the sending end is inputted into the equalizer filter 100, the equalizer filter 100 corrects the received signal to output the same. The outputted signal is inputted into the DD slicer 210 and the Sato slicer 510 connected with the equalizer filter 100.

[037] The DD slicer 210 estimates the original signal from the inputted signal to thus calculate the approximate value, and an abstractor 220 abstracts the value outputted from the equalizer filter 100 from the above calculated value to thus generate a DD error. In order to automatically convert the generated DD error into the Sato error mode, a multiplier 300 multiplies the generated DD error by a scale constant k_1.

[038] The Sato slicer 510 calculates the average value of the original signal from the inputted signal, and an abstractor 520 abstracts the value outputted from the equalizer filter 100 from the calculated average value to thus generate a Sato error. A multiplier 600 multiplies the generated Sato error by a scale constant k_2 in order to automatically convert the Sato error into the DD error mode.

[039] Since the Sato error is larger than the DD error, it has a considerable error value even after it has converged on the optimum point. Therefore, the Sato error value multiplied by the scale constant k_2 is multiplied in a multiplier 700 by the absolute value of the DD error calculated from the DD error size calculation unit 400, and then the result from the multiplier 700 is added in an adder 800 to the DD error value multiplied by the scale constant k_1, whereby it is possible to search the

optimum value of the inverse response of the equalizer. The absolute value of the DD error is obtained by taking the absolute value of the real part and imaginary part of the DD error, respectively.

[040] The above-described G-pseudo update equation and the equation for obtaining the size of the DD error outputted from the DD error size calculation unit 400 will be expressed as follows.

$$e_k^G = k_1 e_k + k_2 |e_k| e_k^S \quad \text{---------- (6)}$$

$$|e_k| = |e_I| + |e_Q| \quad \text{---------- (7)}$$

e_k^G is a G-pseudo error of the current time.

e_K^S is a Sato error of the current time.

e_k is a DD error of the current time.

k_1 and k_2 are scale constants.

e_I is a real error.

e_Q is an imaginary error.

[041] Here, the absolute value of the DD error calculated in the DD error size calculation unit 400 is a value multiplied for correcting the Sato error value as described in Figure 2. If the Sato error value multiplied by the scale constant k_2 is multiplied by the absolute value of the DD error $|e_I| + |e_Q|$, the G-pseudo error is reduced by means of the Sato error only since the DD error has a white value, i.e., uniform value, before t_1. Since the absolute value of the DD error converges on almost 0 after t_1, the Sato error value converges on almost 0 by the G-pseudo update equation for thereby not affecting the G-pseudo error value. Thus, the optimum value of the inverse response of the equalizer is searched by using the DD error value only.

[042] On the other hand, the Sato error has a higher value than the DD error all the time. Thus, although the variation value of the Sato error is small, the size of

the error is larger than that of the Sato error for making error updating dependant upon the Sato error. In this case, the Sato error is multiplied by scale constants k_1 and k_2 so that the size of the first section and the size of the second section are adjusted to a similar size. The scale constants k_1 and k_2 are not predetermined values, but has to be searched by a test. In general, k_1 is set 3-4 times larger than k_2.

[043] Figure 4 is an exemplary view comparing the error distribution by means of the absolute value of a DD error according to the conventional art and the error distribution by means of the absolute value of a DD error according to the present invention.

[044] As illustrated in (A) of Figure ~~4A~~ 4, the error value obtained by adding the square of the real number of the DD error and the square of the imaginary number of the DD error, and taking the square root of the added value has the same value on all points. However, as illustrated in (B) of Figure 4, the absolute value of the real number of the DD error plus the absolute value of the imaginary number of the DD error has a different error value according to a position. In case of (B), though the error value is slightly larger than the error value of (A), it is linearly proportional to the error value of (A).

[045] In the G-pseudo error updating equation according to the conventional art, it can be known that the DD error must not have a precise value, considering the role of the absolute value of the DD error. In other words, if the absolute value of the DD error has an equivalent value to the error value of the conventional art, although it is not identical thereto. If this absolute value is increased or decreased in linear proportion, it has the same effect of using the absolute value of the DD error taking the square root by adjusting k_1 and k_2.

[046] Accordingly, when the DD error size calculation unit ~~24~~ 400 takes the absolute values of the real part and imaginary part, and adds the two values,

i.e., $|e_I| + |e_Q|$, it is possible to obtain the same convergence characteristics as the G-pseudo channel equalizer according to the conventional art, and implement a channel equalizer which has the characteristics of reducing operating time ~~or~~ and complexity.

[047] For example, if a real error and an imaginary error are 10-bits, respectively, it is possible to execute the channel equalizer only in the case that the number of gates of a block is 4960 according to the conventional art. However, the block in which the absolute value of the real error and the absolute value of the imaginary error are added according to the present invention can be implemented by only 292 gates, and it has no difference in its convergence characteristics and its residual error characteristics.

[048] In the combined G-pseudo channel equalizer, the structure of the DD error size calculation unit is modified to thus reduce the number of gates while maintaining the performance of the G-pseudo channel equalizer ~~in the conventional art, and improve~~ and improving error update speed, whereby the complexity of the equalizer is reduced to enhance the performance of the receiver, and the size of a gate block is reduced to decrease the entire size of the receiver.

[049] As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiments are not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the meets and bounds of the claims, or equivalences of such meets and bounds are therefore intended to be embraced by the appended claims.